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EXAMINER	
NGUYEN, VAN THU T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,177	NOGUCHI ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *14-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-13, drawn to error correction and re-write corrected data, classified in class 365, subclass 185.09.

II. Claim 14, drawn to read/write circuitry, classified in class 365, subclass 189.01.

III. Claims 15-20, drawn to associative memory, classified in class 365, subclass 49.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II/III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II/III have separate utility such as they do not require corrected data being rewritten into one of the memory pages. See MPEP § 806.05(d).

3. Inventions II and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as it does not require a temporary memory. See MPEP § 806.05(d).

4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification and fields of search, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Eckhard H. Kuesters on October 20, 2005 a provisional election was made without traverse to prosecute the invention of group I, claims 1-13. Affirmation of this election must be made by applicant in replying to this Office action.

Claims 14-20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

7. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 15, do applicants mean to say --the first memory cells-- instead of "the first memory cell"?

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 12-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Katayama et al. (U.S. Patent No. 6,584,015, hereafter Katayama).

Regarding claim 1, Katayama discloses a data storage system (storage device 101, see FIG. 1) comprising:

a plurality of pages (plurality of blocks in both normal data storing area 104 and substitute data storing area 106, see FIG. 1 and column 3, lines 1-34), each of which includes a plurality of first memory cells (memory cells within each of the blocks), from which at least binary digital data can be read out a plurality of times without destruction of the data (normal data storing area 104 and substitute data storing area 106 are nonvolatile memory);

a circuit (elements performing "identify the error location" task in error detection and correction circuit 109 in FIG. 5, see column 5 lines 55-58) which receives a digital data output (via read out, see FIG. 5) of at least one first page (e.g. block 501) including the first memory cells, detects an error in at least one bit of data, and outputs information on a position of the error; and

a circuit (other elements performing "identify error pattern" task in error detection and correction circuit 109 in FIG. 5, see column 5 lines 55-58) which determines whether the bit of data where the error occurs is "1" or "0" (errors can be only in form of "0" or "1" because memory cells in Katayama store binary data), wherein when a result of the determination is "1" or "0", the first memory cells of the first page is selectively erased and error-corrected data is written therein (corrected data is written back to block 501).

(See column 34-65)

Regarding claim 12, Katayama further discloses, in FIG. 7 in addition with most of the claimed limitations in claim 1, data, which is previously read from block 501 of data storing area 104, is corrected and rewritten into block 701 of data storing area 106.

Regarding claim 13, Katayama discloses, a data storage system comprising:

a plurality of pages (plurality of memory blocks in normal data storing area 104 in FIG. 1), each of which includes a plurality of first memory cells (memory cells within each of the blocks), from which at least binary digital data can be read out a plurality of times without destruction of the data (normal data storing area 104 is nonvolatile)

a plurality of pages (plurality of blocks in normal management area 105 in FIG. 1, and one of them is shown in FIG. 2), each of which includes a plurality of inherent second memory cells (for storing error correction count, block identifier code, etc); and

a circuit (error detection and correction circuit 109 shown in FIG. 2) which receives a digital data output of at least one first page including the first memory cells, and detects an error in at least one bit of data, wherein a plurality of bits of position information on a position of the page where the error occurs is recorded in the second memory cells (e.g. block of logical address 204 shown in FIG. 2).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2-3, 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama in view of Ichige et al. (U.S. Patent No. 6,845,042, hereafter Ichige).

Katayama discloses, as applied in prior rejection of claim 1, all claimed subject matter except further limitations as set forth in claims 2-3, 7-8.

Regarding claims 2-3, Ichige discloses, in FIG. 29, an NAND flash memory device comprising a plurality of pages BLOCK0 to BLOCK1023, each of which including a plurality of first memory cells, e.g. first column of memory cells in the block, and all first columns of all blocks are connected to a data line; and an inherent property of flash memory is that all pages being erased at once.

Since Katayama and Ichige are both from the same field of endeavor, the purpose disclosed by Ichige would have been recognized in the pertinent art of Katayama.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art use the NAND flash memory device disclosed in Ichige for the nonvolatile memory device in Katayama because NAND flash memory is also a nonvolatile memory.

Regarding claim 7, Ichige further discloses, in FIG. 29, wherein the first memory cells comprise a memory cell having a NAND structure where current terminals of the memory cells are serially connected.

Regarding claim 8, Ichige further discloses, in FIG. 30, another AND flash memory having a virtual ground structure where the current terminals of the memory cells are connected in parallel.

Allowable Subject Matter

12. Claims 4-6, 9-11 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowability:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Katayama, Ichige, and Tanzawa et al., taken individually or in combination, do not teach the claimed invention having the following limitations, in combination with the remaining claimed limitations:

(i) **As in claim 4**: wherein in the first memory cells, a plurality of reading operations generate a bit change to a writing state; or

(ii **As in claim 5**: wherein in the first memory cells, the reading operations generate a bit change to a writing state, and determination is selectively made when the bit of data where the error occurs is in an erased state before occurrence of the error; or

(iii) **As in claim 6**: wherein the first memory cell further comprises a charge storage layer of insulating film; or

(iv) **As in claim 9**: wherein if the number of information bits which enables recording of "1" or "0" from the external input/output section is n, and m is a natural number which satisfies $2^{m-1}-1 < n <= 2^{m}-m-1$, the number of memory cells of one page being at least (n+m); or

(v) **As in claim 10**: wherein for the first page including the first memory cells, all information bits can be read out from the external input/output section, and the first page can be read out when power starts to be supplied; or

(vi) **As in claim 11**: wherein the first memory cells comprise a semiconductor memory cell transistor which stores at least three digital values as a plurality of threshold values.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 26, 2005

VanThu Nguyen
Primary Examiner
Art Unit 2824